NVIDIA Jetson Nano Pin and Function Names Guide

Application Note

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Document History

DA-10193-001_v1.0

Version	Date	Authors	Description of Change
1.0	October 20, 2020	BG, SM	Initial Release

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Introduction

The NVIDIA® Jetson Nano™ System on Module (SOM) is built around the NVIDIA® Tegra® X1 System on Chip (SoC). Jetson Nano documentation often refers to names of interfaces, pins, functions, etc., from a SOM perspective. However, other documentation (for example, the TRM) will necessarily take a SoC perspective. Some documentation will reference both SOM and SoC naming. It is important to understand whether a given document is using pin names/numbers, interface names/instances, and function names/instances with reference to the SOM or to the SoC.

Various documents are provided to help customers design, lay out, build, and configure NVIDIA® Jetson™ module-based designs.

Table 1 lists the main documents that are focused on the hardware or contain references to hardware features.

Table 1. Hardware References and Features Documentation

Document Category	Document Name for Jetson Nano Designs	Description
Data Sheet	Jetson Nano Module Data Sheet	• Module overview • Power and system management • Interface and signal description • Electrical, package, and thermal specifications
Technical Reference Manual (TRM)	Tegra X1 SoC Technical Reference Manual	• Address map • Chapters per block (functional description, programming guidelines, and registers)
Product Design Guide	Jetson Nano Product Design Guide	• Power • Interface chapters (connection figures and tables, and routing guidelines)
Carrier Board Specification	Jetson Nano Developer Kit Carrier Board Specification	• Developer Kit features and description • Expansion connector and interface descriptions • Power allocation

Document Category	Document Name for Jetson Nano Designs	Description
Pinmux	Jetson Nano Module Pinmux	• Module pin name and number, SoC ball name • SFIO and GPIO options • Wakes, straps POR state
Design files	Jetson Nano Developer Kit Carrier Board Design Files	• Schematics, layout, bill of materials (BOM) • Misc (Assy drawing, stack-up, gerbers, etc)

Pin and Function Names

There are different pin and interface names in many cases on the module vs. chip. Some documents are based on the chip, such as the TRM, while others are based on the module, or may have both chip and module terms and names. This can lead to confusion. It is important to use the right document and to understand whether a term or name is associated with a chip, module pin name or number, an interface name or instance, or a function name or instance.

Pinmux

The Jetson Nano module pinmux (pin multiplexing) spread sheet has the module pin names and pin numbers in the first two columns, and the SoC ball name in the 3rd column. The GPIOs and SFIO functions are covered in the pin muxing area. The portion of the pinmux in Table 2 includes one of the I2S interfaces.

Table 2. Pinmux I2S and MCLK

		MPIO	Pin Muxing				
Signal Name	**Pin #**	**SoC Ball Name**	**GPIO**	**SFIO0**	**SFIO1**	**SFIO2**	**SFIO3**
GPIO09	211	AUD_MCLK	GPIO3_PBB.00	AUD_MCLK	–	–	–
I2S1_FS	224	DMIC1_CLK	GPIO3_PE.00	–	I2S3_LRCK	–	–
I2S1_DIN	222	DMIC1_DAT	GPIO3_PE.01	–	I2S3_SDATA_IN	–	–
I2S1_DOUT	220	DMIC2_CLK	GPIO3_PE.02	–	I2S3_SDATA_OUT	–	–
I2S1_SCLK	226	DMIC2_DAT	GPIO3_PE.03	–	I2S3_SCLK	–	–

In the case shown in Table 2, for one of the I2S interfaces that are available on the module pins, the following pin/function names exist:

- Module signal names: I2S1_xxx
- SoC chip pin names: DMIC[2:1]_xxx
- SFIO 0 function names: I2S3_xxx

This shows that the module pin names, chip pin names, and function names can be different. When referring to the various documents, it is important to understand which name form is applicable. For instance, if the TRM is accessed for information on how to configure the pins or functions, it is necessary to know that the TRM is chip focused. It will have SoC pin names when referring to the pins, such as in the "Pinmux Register" section, or function names if the function is being configured. In the case of the module data sheet, the module pin names are relevant. See the following "TRM" and "Data Sheet" sections for details.

Data Sheet

The module data sheet only uses the module pin names. If a programmer needed to know what SoC function to configure, it would be necessary to look at either the pinmux spreadsheet or product design guide to know what SoC function is associated with that module pin.

Table 3. Data Sheet I2S1 and MCLK Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
211	GPIO09	GPIO #9 or Audio Codec Master Clock	Bidir	CMOS – 1.8V
226	I2S1_SCLK	I2S Audio Port 1 Clock	Bidir	CMOS – 1.8V
224	I2S1_FS	I2S Audio Port 1 Left/Right Clock	Bidir	CMOS – 1.8V
220	I2S1_DOUT	I2S Audio Port 1 Data Out	Output	CMOS – 1.8V
222	I2S1_DIN	I2S Audio Port 1 Data In	Input	CMOS – 1.8V

Technical Reference Manual

The technical reference manual (TRM) is based on the chip (for example, Tegra X1). References to pin names (such as DAP4) will be chip pin names. There are also references to functions (such as I2S1). These should match the names of functions in the pinmux spreadsheet or product design guide. To know what pin on the module an SoC pin is associated with, the pinmux spreadsheet is the best cross reference, although the product design guide has that information as well.

9.15.39 PINMUX_AUX_DMIC1_CLK_0

Offset: 0x30a4 | Read/Write: R/W | Reset: 0x00000074 (0bxxxxxxxxxxxxxxxxxxxx00xx001110100)

Bit	Reset	Description
1:0	DMIC1	PM: 0 = DMIC1 1 = I2S3 2 = RSVD2 3 = RSVD3

Product Design Guide

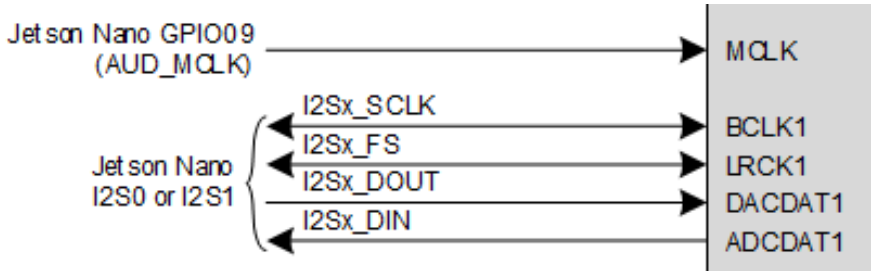
The product design guide focuses on the module, but many of the figures and pin description tables also include the SoC signal associated with a module pin where applicable. The partial table contains the same I2S interface used as the example in the earlier document sections. Both the module (Jetson Nano) and SoC pin names are shown.

Table 4. Jetson Nano Audio Pin Description

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
211	GPIO09	AUD_MCLK	GPIO #9 or Audio Codec Master Clock	Expansion Header	Output	CMOS – 1.8V	ST	pd
226	I2S1_SCLK	DMIC2_DAT	I2S Audio Port 1 Clock		Bidir		ST	pd
224	I2S1_FS	DMIC1_CLK	I2S Audio Port 1 Left/Right Clock		Bidir		ST	pd
220	I2S1_DOUT	DMIC2_CLK	I2S Audio Port 1 Data Out		Output		ST	pd
222	I2S1_DIN	DMIC1_DAT	I2S Audio Port 1 Data In		Input		ST	pd

Figure 1 also shows the I2S interface connected to an Audio Codec and includes the module pin names and Codec pin names.

Figure 1. I2S0 or I2S1 Interface Connections to Codec



The following audio connections table contains only the module pin names, or function names in parenthesis if necessary, for clarity.

Table 5. Audio Signal Connections

Module Pin Name	Type	Termination	Description
I2S[1:0]_SCLK	I/O		I2S Serial Clock: Connect to I2S/PCM CLK pin of audio device.
I2S[1:0]_FS	I/O		I2S Frame Select (Left/Right Clock): Connect to corresponding pin of audio device.
I2S[1:0]_DOUT	I/O		I2S Data Output: Connect to data input pin of audio device.
I2S[1:0]_DIN	I		I2S Data Input: Connect to data output pin of audio device.
GPIO09	O		Audio Codec Master Clock: Connect to clock pin of audio codec.

Developer Kit Carrier Board Specification

The developer kit specification uses module (Jetson Nano) pin names and pin numbers from the carrier board reference design. If it is necessary to know the corresponding SoC name or function, the pinmux should be referenced (the design guide also contains this information).

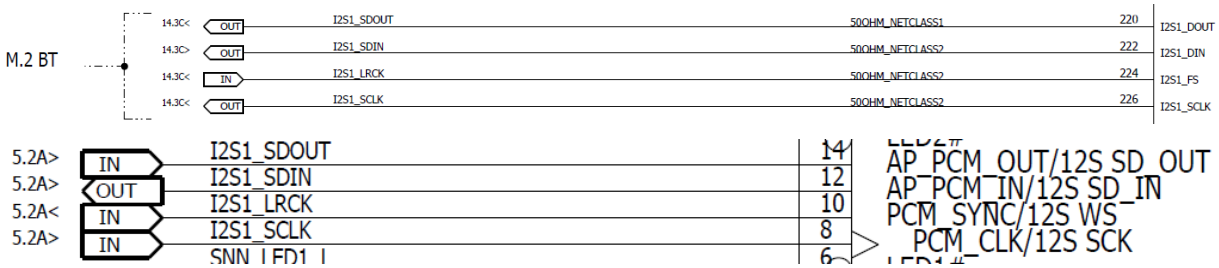
Table 6. I2S Connections to M.2 Key E Socket on Carrier Board

Pin # (M.2)	Module Pin Name	Usage/Description	Type/Dir
8	I2S1_CLK	I2S #1 Clock	Bidir
10	I2S1_FS	I2S #1 Left/Right Clock	Bidir
12	I2S1_DIN	I2S #1 Data In	Input
14	I2S1_DOUT	I2S #1 Data Out	Output

Design Files

The design files (schematics, layout, etc.) also contain only module pin names and net names. Look to the pinmux or product design guide if it is necessary to know which chip pin is associated with a module pin name.

Figure 2. Design Schematics



Chip, Module, and Carrier Board Pin Names and Numbers

The information provided in the following table can be found in various hardware documentation (as described within this application note). Table 7 provides a consolidation of this information for your convenience.

Table 7. Chip, Module, and Carrier Board Pinout – Odd Row

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
1	GND	GND	–
3	CSI1_D0_N	CSI1_D0_N	CSI_B_D0_N
5	CSI1_D0_P	CSI1_D0_P	CSI_B_D0_P
7	GND	GND	–
9	RSVD	–	–
11	RSVD	–	–
13	GND	GND	–
15	CSI1_D1_N	CSI1_D1_N	CSI_B_D1_N
17	CSI1_D1_P	CSI1_D1_P	CSI_B_D1_P
19	GND	GND	–
21	CSI3_D0_N	CSI3_D0_N	CSI_F_D0_N
23	CSI3_D0_P	CSI3_D0_P	CSI_F_D0_P
25	GND	GND	–
27	CSI3_CLK_N	CSI3_CLK_N	CSI_F_CLK_N
29	CSI3_CLK_P	CSI3_CLK_P	CSI_F_CLK_P
31	GND	GND	–
33	CSI3_D1_N	CSI3_D1_N	CSI_F_D1_N
35	CSI3_D1_P	CSI3_D1_P	CSI_F_D1_P
37	GND	GND	–
39	DP0_TXD0_N	DP0_TXD0_N	EDP_TXDN0
41	DP0_TXD0_P	DP0_TXD0_P	EDP_TXDP0

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
43	GND	GND	–
45	DP0_TXD1_N	DP0_TXD1_N	EDP_TXDN1
47	DP0_TXD1_P	DP0_TXD1_P	EDP_TXDP1
49	GND	GND	–
51	DP0_TXD2_N	DP0_TXD2_N	EDP_TXDN2
53	DP0_TXD2_P	DP0_TXD2_P	EDP_TXDP2
55	GND	GND	–
57	DP0_TXD3_N	DP0_TXD3_N	EDP_TXDN3
59	DP0_TXD3_P	DP0_TXD3_P	EDP_TXDP3
61	GND	GND	–
63	DP1_TXD0_N	HDMI_TX2_N	HDMI_DP_TXDN0
65	DP1_TXD0_P	HDMI_TX2_P	HDMI_DP_TXDP0
67	GND	GND	–
69	DP1_TXD1_N	HDMI_TX1_N	HDMI_DP_TXDN1
71	DP1_TXD1_P	HDMI_TX1_P	HDMI_DP_TXDP1
73	GND	GND	–
75	DP1_TXD2_N	HDMI_TX0_N	HDMI_DP_TXDN2
77	DP1_TXD2_P	HDMI_TX0_P	HDMI_DP_TXDP2
79	GND	GND	–
81	DP1_TXD3_N	HDMI_TXC_N	HDMI_DP_TXDN3
83	DP1_TXD3_P	HDMI_TXC_P	HDMI_DP_TXDP3
85	GND	GND	–
87	GPIO00	USB0_VBUS_DET*	USB_VBUS_EN0
89	SPI0_MOSI	SPI0_MOSI	SPI1_MOSI
91	SPI0_SCK	SPI0_SCK	SPI1_SCK
93	SPI0_MISO	SPI0_MISO	SPI1_MISO
95	SPI0_CS0*	SPI0_CS0	SPI1_CS0
97	SPI0_CS1*	SPI0_CS1	SPI1_CS1
99	UART0_TXD	UART0_TXD	UART3_TXD
101	UART0_RXD	UART0_RXD	UART3_RXD
103	UART0_RTS*	UART0_RTS	UART3_RTS
105	UART0_CTS*	UART0_CTS	UART3_CTS
107	GND	GND	–
109	USB0_D_N	USB0_AP_N	USB0_DN
111	USB0_D_P	USB0_AP_P	USB0_DP
113	GND	GND	–
115	USB1_D_N	USB1_AP_N	USB1_DN

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
117	USB1_D_P	USB1_AP_P	USB1_DP
119	GND	GND	–
121	USB2_D_N	USB2_AP_N	USB2_DN
123	USB2_D_P	USB2_AP_P	USB2_DP
125	GND	GND	–
127	GPIO04	PWR_LED_CTRL	NFC_INT
129	GND	GND	–
131	PCIE0_RX0_N	PCIE0_RX0_M2_N	PEX_RX4N
133	PCIE0_RX0_P	PCIE0_RX0_M2_P	PEX_RX4P
135	GND	GND	–
137	PCIE0_RX1_N	PCIE0_RX1_N	PEX_RX3N
139	PCIE0_RX1_P	PCIE0_RX1_P	PEX_RX3P
141	GND	GND	–
143	RSVD	–	–
145	RSVD	–	–
147	GND	GND	–
149	PCIE0_RX2_N	PCIE0_RX2_N	PEX_RX2N
151	PCIE0_RX2_P	PCIE0_RX2_P	PEX_RX2P
153	GND	GND	–
155	PCIE0_RX3_N	PCIE0_RX3_N	PEX_RX1N
157	PCIE0_RX3_P	PCIE0_RX3_P	PEX_RX1P
159	GND	GND	–
161	USBSS_RX_N	USBSS_TX6_HUB_N	PEX_RX6N
163	USBSS_RX_P	USBSS_TX6_HUB_P	PEX_RX6P
165	GND	GND	–
167	RSVD	–	–
169	RSVD	–	–
171	GND	GND	–
173	RSVD	–	–
175	RSVD	–	–
177	GND	GND	–
179	PCIE_WAKE*	PCIE_WAKE	PEX_WAKE_N
181	PCIE0_RST*	PCIE0_RST	PEX_L0_RST_N
183	RSVD	–	–
185	I2C0_SCL	ID_I2C_SCL	GEN1_I2C_SCL
187	I2C0_SDA	ID_I2C_SDA	GEN1_I2C_SDA
189	I2C1_SCL	I2C1_SCL	GEN2_I2C_SCL

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
191	I2C1_SDA	I2C1_SDA	GEN2_I2C_SDA
193	I2S0_DOUT	I2S0_SDOUT	DAP4_DOUT
195	I2S0_DIN	I2S0_SDIN	DAP4_DIN
197	I2S0_FS	I2S0_LRCK	DAP4_FS
199	I2S0_SCLK	I2S0_SCLK	DAP4_SCLK
201	GND	GND	–
203	UART1_TXD	UART1_TXD	UART2_TXD
205	UART1_RXD	UART1_RXD	UART2_RXD
207	UART1_RTS*	UART1_RTS	UART2_RTS
209	UART1_CTS*	UART1_CTS	UART2_CTS
211	GPIO09	GPIO09	AUD_MCLK
213	CAM_I2C_SCL	CAM_I2C_SCL	CAM_I2C_SCL
215	CAM_I2C_SDA	CAM_I2C_SDA	CAM_I2C_SDA
217	GND	GND	–
219	SDMMC_DAT0	SDIO_D0	SDMMC3_DAT0
221	SDMMC_DAT1	SDIO_D1	SDMMC3_DAT1
223	SDMMC_DAT2	SDIO_D2	SDMMC3_DAT2
225	SDMMC_DAT3	SDIO_D3	SDMMC3_DAT3
227	SDMMC_CMD	SDIO_CMD	SDMMC3_CMD
229	SDMMC_CLK	SDIO_CLK	SDMMC3_CLK
231	GND	GND	–
233	SHUTDOWN_REQ*	FORCE_OFF*	–
235	PMIC_BBAT	BBAT	(PMIC BBATT)
237	POWER_EN	POWER_EN	(PMIC EN0 through converter logic)
239	SYS_RESET*	SYS_RST*	SYS_RESET_IN_N
241	GND	GND	–
243	GND	GND	–
245	GND	GND	–
247	GND	GND	–
249	GND	GND	–
251	VDD_IN	VDD_5V_IN	–
253	VDD_IN	VDD_5V_IN	–
255	VDD_IN	VDD_5V_IN	–
257	VDD_IN	VDD_5V_IN	–
259	VDD_IN	VDD_5V_IN	–

Table 8. Chip, Module, and Carrier Board Pinout – Even Row

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
2	GND	GND	–
4	CSI0_D0_N	CSI0_D0_N	CSI_A_D0_N
6	CSI0_D0_P	CSI0_D0_P	CSI_A_D0_P
8	GND	GND	–
10	CSI0_CLK_N	CSI0_CLK_N	CSI_A_CLK_N
12	CSI0_CLK_P	CSI0_CLK_P	CSI_A_CLK_P
14	GND	GND	–
16	CSI0_D1_N	CSI0_D1_N	CSI_A_D1_N
18	CSI0_D1_P	CSI0_D1_P	CSI_A_D1_P
20	GND	GND	–
22	CSI2_D0_N	CSI2_D0_N	CSI_E_D0_N
24	CSI2_D0_P	CSI2_D0_P	CSI_E_D0_P
26	GND	GND	–
28	CSI2_CLK_N	CSI2_CLK_N	CSI_E_CLK_N
30	CSI2_CLK_P	CSI2_CLK_P	CSI_E_CLK_P
32	GND	GND	–
34	CSI2_D1_N	CSI2_D1_N	CSI_E_D1_N
36	CSI2_D1_P	CSI2_D1_P	CSI_E_D1_P
38	GND	GND	–
40	CSI4_D2_N	CSI4_D2_N	CSI_D_D0_N
42	CSI4_D2_P	CSI4_D2_P	CSI_D_D0_P
44	GND	GND	–
46	CSI4_D0_N	CSI4_D0_N	CSI_C_D0_N
48	CSI4_D0_P	CSI4_D0_P	CSI_C_D0_P
50	GND	GND	–
52	CSI4_CLK_N	CSI4_CLK_N	CSI_C_CLK_N
54	CSI4_CLK_P	CSI4_CLK_P	CSI_C_CLK_P
56	GND	GND	–
58	CSI4_D1_N	CSI4_D1_N	CSI_C_D1_N
60	CSI4_D1_P	CSI4_D1_P	CSI_C_D1_P
62	GND	GND	–
64	CSI4_D3_N	CSI4_D3_N	CSI_D_D1_N
66	CSI4_D3_P	CSI4_D3_P	CSI_D_D1_P
68	GND	GND	–
70	DSI_D0_N	DSI_D0_N	DSI_A_D0_N
72	DSI_D0_P	DSI_D0_P	DSI_A_D0_P

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
74	GND	GND	–
76	DSI_CLK_N	DSI_CLK_N	DSI_A_CLK_N
78	DSI_CLK_P	DSI_CLK_P	DSI_A_CLK_P
80	GND	GND	–
82	DSI_D1_N	DSI_D1_N	DSI_A_D1_N
84	DSI_D1_P	DSI_D1_P	DSI_A_D1_P
86	GND	GND	–
88	DP0_HPD	DP0_HPD	DP_HPD0
90	DP0_AUX_N	DP0_AUX_N	DP_AUX_CH0_N
92	DP0_AUX_P	DP0_AUX_P	DP_AUX_CH0_P
94	HDMI_CEC	HDMI_CEC	HDMI_CEC
96	DP1_HPD	HDMI_HPD	HDMI_INT_DP_HPD
98	DP1_AUX_N	HDMI_DDC_SDA_POL	DP_AUX_CH1_N
100	DP1_AUX_P	HDMI_DDC_SCL_POL	DP_AUX_CH1_P
102	GND	GND	–
104	SPI1_MOSI	SPI1_MOSI	SPI2_MOSI
106	SPI1_SCK	SPI1_SCK	SPI2_SCK
108	SPI1_MISO	SPI1_MISO	SPI2_MISO
110	SPI1_CS0*	SPI1_CS0	SPI2_CS0
112	SPI1_CS1*	SPI1_CS1	SPI2_CS1
114	CAM0_PWDN	CAM0_PWDN	CAM1_PWDN
116	CAM0_MCLK	CAM0_MCLK	CAM1_MCLK
118	GPIO01	GPIO01	CAM_AF_EN
120	CAM1_PWDN	CAM1_PWDN	CAM2_PWDN
122	CAM1_MCLK	CAM1_MCLK	CAM2_MCLK
124	GPIO02	BT_M2_WAKE_AP	GPIO_PH6
126	GPIO03	BT_M2_EN	GPS_EN
128	GPIO05	W_DISABLE1_CTRL	AP_WAKE_NFC
130	GPIO06	CAM_MUX_SEL	NFC_EN
132	GND	GND	–
134	PCIE0_TX0_N	PCIE0_TX0_AP_N	PEX_TX4N
136	PCIE0_TX0_P	PCIE0_TX0_AP_P	PEX_TX4P
138	GND	GND	–
140	PCIE0_TX1_N	PCIE0_TX1_N	PEX_TX3N
142	PCIE0_TX1_P	PCIE0_TX1_P	PEX_TX3P
144	GND	GND	–
146	GND	GND	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
148	PCIE0_TX2_N	PCIE0_TX2_N	PEX_TX2N
150	PCIE0_TX2_P	PCIE0_TX2_P	PEX_TX2P
152	GND	GND	–
154	PCIE0_TX3_N	PCIE0_TX3_N	PEX_TX1N
156	PCIE0_TX3_P	PCIE0_TX3_P	PEX_TX1P
158	GND	GND	–
160	PCIE0_CLK_N	PCIE0_CLK_N	PEX_CLK1N
162	PCIE0_CLK_P	PCIE0_CLK_P	PEX_CLK1P
164	GND	GND	–
166	USBSS_TX_N	USBSS_TX6_N	PEX_TX6N
168	USBSS_TX_P	USBSS_TX6_P	PEX_TX6P
170	GND	GND	–
172	RSVD	–	–
174	RSVD	–	–
176	GND	GND	–
178	MOD_SLEEP*	MOD_SLEEP*	GPIO_PA6
180	PCIE0_CLKREQ*	PCIE0_CLKREQ	PEX_L0_CLKREQ_N
182	RSVD	–	–
184	GBE_MDI0_N	GBE_MDI0_N	–
186	GBE_MDI0_P	GBE_MDI0_P	–
188	GBE_LED_LINK	GBE_LED_LINK	–
190	GBE_MDI1_N	GBE_MDI1_N	–
192	GBE_MDI1_P	GBE_MDI1_P	–
194	GBE_LED_ACT	GBE_LED_ACT	–
196	GBE_MDI2_N	GBE_MDI2_N	–
198	GBE_MDI2_P	GBE_MDI2_P	–
200	GND	GND	–
202	GBE_MDI3_N	GBE_MDI3_N	–
204	GBE_MDI3_P	GBE_MDI3_P	–
206	GPIO07	GPIO07	LCD_BL_PWM
208	GPIO08	FAN_TACH	GPIO_PZ2
210	CLK_32K_OUT	SUSCLK_32KHZ	(PMIC GPIO4 32K CLK Out)
212	GPIO10	M2E_ALERT*	LCD_BL_EN
214	FORCE_RECOVERY*	FORCE_RECOVERY*	BUTTON_VOL_UP
216	GPIO11	GPIO11	GPIO_PZ0
218	GPIO12	GPIO12	LCD_TE
220	I2S1_DOUT	I2S1_SDOUT	DMIC2_CLK

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
222	I2S1_DIN	I2S1_SDIN	DMIC1_DAT
224	I2S1_FS	I2S1_LRCK	DMIC1_CLK
226	I2S1_SCLK	I2S1_SCLK	DMIC2_DAT
228	GPIO13	GPIO13	GPIO_PE6
230	GPIO14	FAN_PWM	GPIO_PE7
232	I2C2_SCL	I2C2_SCL	GEN3_I2C_SCL
234	I2C2_SDA	I2C2_SDA	GEN3_I2C_SDA
236	UART2_TXD	UART2_TXD	UART1_TXD
238	UART2_RXD	UART2_RXD	UART1_RXD
240	SLEEP/WAKE*	PWR_BTN*	BUTTON_POWER_ON
242	GND	GND	–
244	GND	GND	–
246	GND	GND	–
248	GND	GND	–
250	GND	GND	–
252	VDD_IN	VDD_5V_IN	–
254	VDD_IN	VDD_5V_IN	–
256	VDD_IN	VDD_5V_IN	–
258	VDD_IN	VDD_5V_IN	–
260	VDD_IN	VDD_5V_IN	–

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